

Abstract

With the increased number of embedded memories in mobile devices, minimizing the test power becomes a serious concern, especially when parallel testing is applied. Battery will be lost and the entire System on Chip (SoC) is subjected to be damaged if the consumed power exceeds the power constraint of the chip.

This dissertation proposes a number of techniques to address these challenges during memory testing. The first technique is based on using low power Linear Feedback Shift Register (LFSR) as an address generator when applying Zero-One algorithm during Memory Built-in Self Test (MBIST), and then, re-order the test so that total switching activity in address decoder and write driver is minimized. The obtained results show that up to 60% reduction in switching activity can be achieved during testing large size memories with negligible overhead in hardware area.

Another technique that aims to reduce average and peak power during March tests is proposed. In this technique, the word of the Memory Under Testing (MUT) is divided into two clusters so that write operation is applied just to one cluster. Obtained results show that around 42% reduction in peak power and around 35% reduction in average power can be achieved using the proposed technique with the same fault coverage and testing time of original tests.

Finally, a new scheme is proposed to manage parallel testing of large number of embedded memories in SoC. This scheme is based on grouping different memories into clusters based on their word lengths and scheduling read and write operations in such a way that the consumed power is optimal. Simulation results of case-of-study show that up to 60% reduction in peak power can be achieved in case of parallel testing at a cost of only one additional clock cycle in testing time